Broad-Band Medium-Power Amplification in the 2–12.4-GHz Range with GaAs MESFET's

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Abstract—**The design of 100-mW GaAs MESFET amplifiers for the 2–6.2-GHz and 5.9–12.4-GHz bands is described. Both small-signal and large-signal matching considerations are presented to obtain a minimum 10-dB gain using a 1-μm GaAs MESFET. Three combination techniques, direct paralleling, resistive combiners, and hybrid quadrature couplers are discussed. Finally, considerations for absolute stability are presented.**

I. Introduction

MOST of the emphasis in GaAs MESFET amplifier design to date has been on broad-band low-noise designs [1]–[3] and on narrow-band high-power amplifiers with as much as a watt output [4]. This paper describes the development of amplifiers aimed at combining medium power and very broad bandwidths. Typical performance is 100-mW output over bandwidths up to 3.1:1. The specified frequency ranges for the amplifiers described are 2–6.2 GHz and 5.9–12.4 GHz, with correspondingly larger design bandwidths to allow for production variations, environmental degradations, and design margin. Each amplifier has a nominal 10-dB gain, and reflection coefficients less than 0.3 at both input and output. Noise performance was not a consideration in the design of these amplifiers.

II. GaAs MESFET

The GaAs MESFET used in the two amplifier designs discussed is essentially the device described by Liechti and Tillman [1]. An epitaxial layer, 0.2 μm thick and doped 1×10^{17} cm^{-3}, is grown on a semi-insulating substrate. A metal gate stripe 1 μm wide and 500 μm long is deposited between source and drain Au–Ge ohmic contacts. The entire MESFET chip measures 0.635 × 0.254 × 0.127 mm. This GaAs MESFET can be represented by the equivalent circuit of Fig. 1, the calculated performance of which agrees well with measured parameters at dc and 1 MHz and with measured microwave S-parameters [2].

III. Amplifier Design

Both small-signal and large-signal techniques were used to optimize gain, bandwidth, and output power. A single MESFET with both input and output matched for small-signal gain at 10 GHz shows typically 16 dBm at a 1-dB compression point [Fig. 2(a)]. However, by optimizing the drain match for saturated power, small-signal gain can be compromised for increased large-signal gain [Fig. 2(b)]. At these large-signal levels, optimum gate bias is negative by as much as 1–2 V. Typically, as shown in Fig. 2(c), an optimum gate bias and drain matching circuit for large signal will cause a 2–3-dB loss in small-signal gain but a corresponding 4-dB increase in output power at the 1-dB compression point. Therefore, the following small-signal techniques were used to optimize preamplifier stages and the gate matching circuits of the power stage. Measured large-signal data were used to optimize the output drain circuitry.

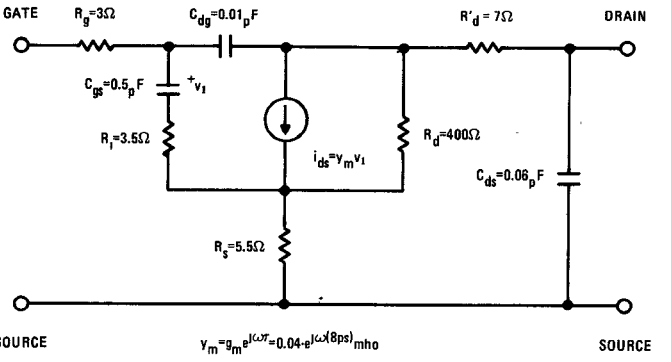

Fig. 1. GaAs MESFET model with typical element values.

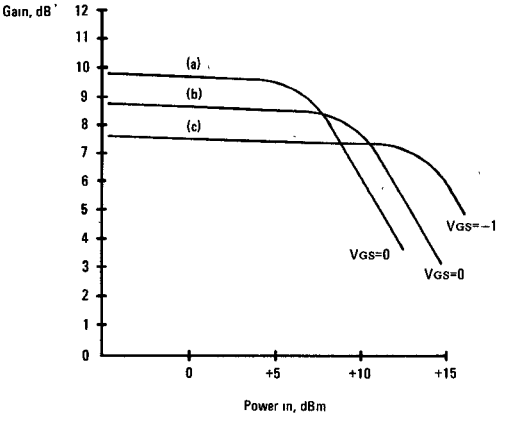

Fig. 2. Gain versus power in for common source GaAs MESFET at 10 GHz, I_{DSS} = 100 mA. (a) Both input and output matched for small-signal gain, V_{GS} = 0. (b) Input matched for small-signal gain, output matched for large-signal gain, V_{GS} = 0. (c) Input matched for small-signal gain, output match and gate bias optimized for large-signal gain. Condition (c) at 1-dB compression yields 30.5-percent power-added efficiency.

A. Small-Signal Matching

The design sequence for both 2–6.2-GHz and 5.9–12.4-GHz amplifiers was to use a unilateral approximation to form simplified input and output equivalents to the MESFET, choose an appropriate low-pass prototype matching structure, and finally use computer optimization and modeling for MIC implementation. For matching calculations, the model of Fig. 1 may be approximated by a series RC

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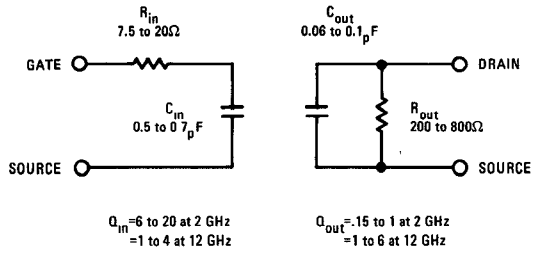

Fig. 3. GaAs MESFET input and output simplified equivalents.

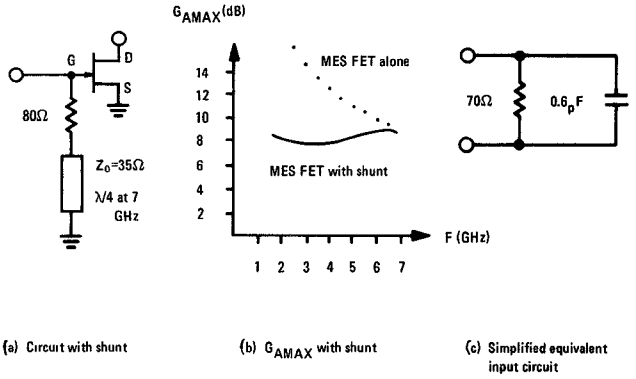

Fig. 4. Shunted MESFET input for 2–6.2-GHz amplifier. (a) Circuit with shunt. (b) $G_{A\,max}$ with shunt. (c) Simplified equivalent for shunted MESFET. Range of values shown represent expected device-to-device variations.

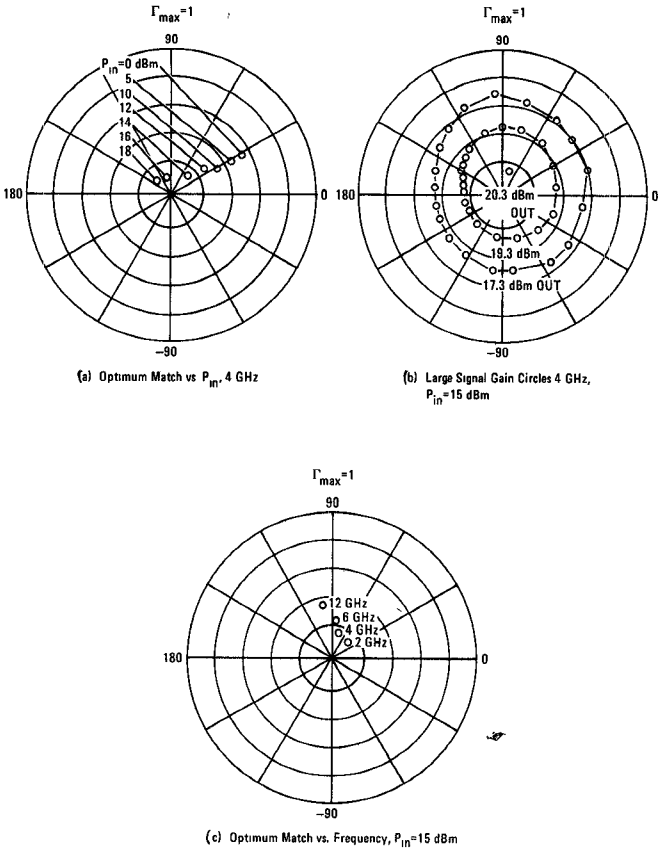

Fig. 5. Typical large-signal match measurements, $Z_{ref} = 50\ \Omega$. (a) Optimum match versus P_{in}, 4 GHz. (b) Large-signal gain circles at 4 GHz, $P_{in} = 15$ dBm. (c) Optimum match versus frequency, $P_{in} = 15$ dBm.

circuit representing the input and a parallel *RC* circuit for the output as shown in Fig. 3.

Comparison of the two design approaches are worth noting. Due to the high input Q and the feasibility of lumped design techniques for the 2–6.2 amplifier, a resistive loaded shunt network was added at the gate (Fig. 4) to decrease the input Q without greatly reducing the maximum available gain, $G_{A\,max}$, at 6 GHz. Other advantages of this approach are flat $G_{A\,max}$ and simple equivalent circuit in the frequency band of interest.

Matching circuits for the shunted MESFET were designed in lumped low-pass filter form using the techniques of Matthaei [5], Levy [6], and Fano [7]. It was necessary to use Fano's results for an analytical approach to matching the shunted GaAs MESFET input because the 0.6-pF capacitance (Fig. 4) was too large to incorporate in the usual impedance transforming configurations. The other references noted were suitable and more convenient for use in output matching synthesis. Circuits were then computer simulated in distributed form with parasitics to finalize the design.

For the 5.9–12.4-GHz amplifier, circuit elements had to be represented in distributed form, and parasitics were more important and less predictable. A typical design approach was to convert a lumped low-pass filter form to an approximate distributed topology for a starting point. This distributed topology was then optimized by the computer [8] within constraints consistent with microstrip on 0.25-mm-thick sapphire. Parasitics such as chip capacitor pads, bonding wires, and large impedance steps were modeled based on available design data [9]–[11].

This distributed modeling approach along with careful *S*-parameter measurements of matching circuits to check predicted design results gave single-stage MESFET amplifier prototypes meeting design goals with no circuit adjustments. A slight amount of tuning near drain bonding wires was incorporated in the three-stage amplifiers to compensate for a variable inductance introduced because of mechanical tolerances in the circuit carrier.

B. Large-Signal Matching

The final stage output matching circuit of each amplifier was designed for optimum power output rather than small-signal match. A series of experiments was used to measure large-signal match. The optimum load was determined by adjusting an output tuner for maximum power and then measuring the impedance presented by the tuner to the MESFET drain. Large-signal gain circles and plots of optimum load versus P_{in} were obtained in this way (Fig. 5). These measurements agree with predictions based simply on the dc drain characteristics of the MESFET—namely, that the real part of the load for maximum power output should be nearly independent of frequency, with a conductive component on the order of $F_{DS}/V_{DD} \simeq 100$ mA/5 V = 20 mmho at high power levels.

C. Combining Techniques

To obtain the required 20-dBm output level over a 3:1 bandwidth, it was necessary to combine the output of two MESFET's, each capable of delivering 17–18-dBm minimum with optimum large-signal match. The least lossy combining

method was direct paralleling, which consisted of bonding the gate and drain contacts of two chips together, then treating these chips with bond parasitics as a single common source device.

For the 2–6.2-GHz amplifier, quadrature hybrids and symmetrical resistive splitters were investigated as combining techniques in addition to direct paralleling. The advantages of couplers are: easier broad-band matching to individual MESFET's than to parallel MESFET's; and, for quadrature couplers, the attendant amplifier improvements described by Kurokawa [12]. The disadvantages are additional losses and larger, more costly circuits.

Resistive splitters were found to have little advantage over direct paralleling for combining power from two MESFET's, and they added about 0.5-dB loss. However, they were straightforward to fabricate from readily available design data [13] and flat to within a few tenths of a decibel over 2–8 GHz.

Interdigitated quadrature couplers [14] required more design effort but did give the expected performance improvements. While the power split is not as constant across the band in the interdigitated coupler as in the power splitter, the almost exact phase quarature across the band provides for a well-balanced operation and results in improved input and output match. Input and output return loss increased from 5 to 20 dB over similar designs with splitters or parallel MESFET's, to 17-dB minimum (2–6.2 GHz) at the input, and 13-dB minimum at the output under large-signal (20-dBm out) conditions. Losses and coupling imbalance resulted in as much as 2-dB lower power output capability than other combining techniques. Output power of 20 dBm minimum was achieved with MESFET chips with $I_{DSS} > 70$ mA.

For the 5.9–12.4-GHz amplifier, the low saturated gain of the MESFET's precluded the use of couplers. Direct paralleling was used to obtain 20 dBm out of the final stage with 3-dB gain. To obtain this level of performance at 12.4 GHz, it was necessary to use MESFET's with similar values of C_{gs} and to individually adjust each gate bias voltage.

The gate input of the parallel MESFET can be described as two parallel admittances. For the case of $R_1 \neq R_2$ and $C_1 \neq C_2$ a nonsymmetrical current flow can occur. Amplifiers with mismatched values of C_{in} in the range of 0.5–0.7 pF with a fixed large-signal input gave power gains consistent with the matched C_{in} to within 0.5 dB. However, greater than 0.4-pF mismatches in C_{in} showed as much as 1.8-dB lower large-signal gain than with matched chips.

At large-signal levels, gate bias for maximum power gain will be in the range of 0 to -2 V. Individual gate biasing on the parallel MESFET combination optimizes the operating point and provides up to 1-dB greater gain. A single drain bias line is used, however, since power output increases monotonically with V_{DS}.

D. Stability

From dc to about 4 GHz, the GaAs MESFET modeled in Fig. 1 can be made to oscillate if the impedance presented to the gate is high enough. The potential instability is due to feedback through the gate to drain capacitance, C_{gd}. Since the feedback reactance varies as $1/\omega$, the input impedance required for potential instability increases without bound as the frequency approaches zero. Stability factor calculations based on the model of Fig. 1 show that 1 MΩ from gate to ground results in unconditional stability from dc to about 1 MHz; 1 kΩ from gate to ground gives unconditional stability from dc to 1 GHz. A gate-to-ground resistance of about 200 Ω or less would be desirable in an amplifier for stability at all frequencies, allowing for device variations and a conservative design margin. However, a resistance of 2 kΩ or more is desirable for self-biasing a power amplifier and providing automatic protection against excessive gate currents during heavy overdrive. For simplicity and reliability, it was decided to self-bias the amplifiers with 2 kΩ from gate to ground. This was implemented by placing dc blocking on shunted RF elements and placing a 2-kΩ series resistance in the gate bias line. In the frequency range where this configuration alone is not unconditionally stable, the remaining matching circuitry is chosen to assure unconditional stability.

Above 4 GHz the intrinsic MESFET is unconditionally stable in a common source configuration. However, inductances of a few tenths of a nanohenry in the common source lead can cause potential instability at X-band frequencies and above. By using four to six source bonds of under 0.13-mm length, the source inductance was held to about 0.05 nH and such oscillations were eliminated.

An anomalous low-level ($\simeq -60$-dBm) oscillation was observed on certain MESFET wafers. The frequency spectrum contained numerous spikes, not harmonically related, ranging from low-megahertz to X-band frequencies, as well as a broad-band noise floor. The occurrence of oscillations was sensitive to drain and gate voltages, occurring at the higher drain voltages but ceasing as the gate was reverse biased. This is evidently Gunn oscillation, as noted by Turner *et al.* [15]. This premise was substantiated by shorting the gate directly to the source with a short bond and using low-inductance (< 0.05-nH) source bonds. The oscillation was still present under these conditions (short-circuit gate unstable) which ruled out low- and high-frequency feedback instability mentioned earlier. The oscillation frequency was tuneable from typically 10 GHz to 6.5 GHz with $V_{DS} = 3$–5 V. Fortunately, this oscillation was completely attenuated with gate reverse bias on the order of 0.5 V or less and was not present with normal optimum large-signal biases.

Circuit configurations and electrical performance of the 2–6.2- and 5.9–12.4-GHz amplifiers are shown in Figs. 6 and 7, respectively. Actual MIC layout of the 2–6.2 amplifier output stage (Fig. 8) shows two single MESFET stages combined with interdigitated quadrature couplers. A single 2–6.2-GHz MESFET driver stage was used to obtain 10-dB gain at 100-mW output. The entire three-stage 5.9–12.4 layout using direct parallel MESFET stages is shown in Fig. 9. This configuration yielded 4-dB minimum driver stages with a 3-dB power stage to meet the minimum goal of

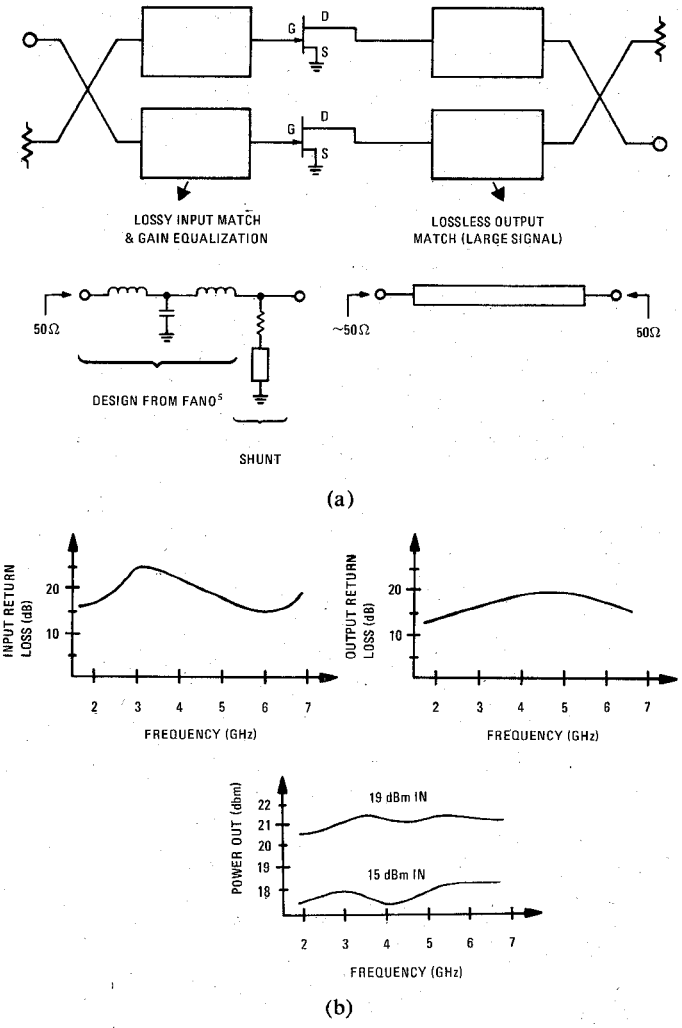

Fig. 6. Output stage of 100 mW, 2–6.2-GHz GaAs MESFET amplifier. (a) Output stage block diagram. (b) Output stage input return loss, output return loss, and output power performance versus frequency.

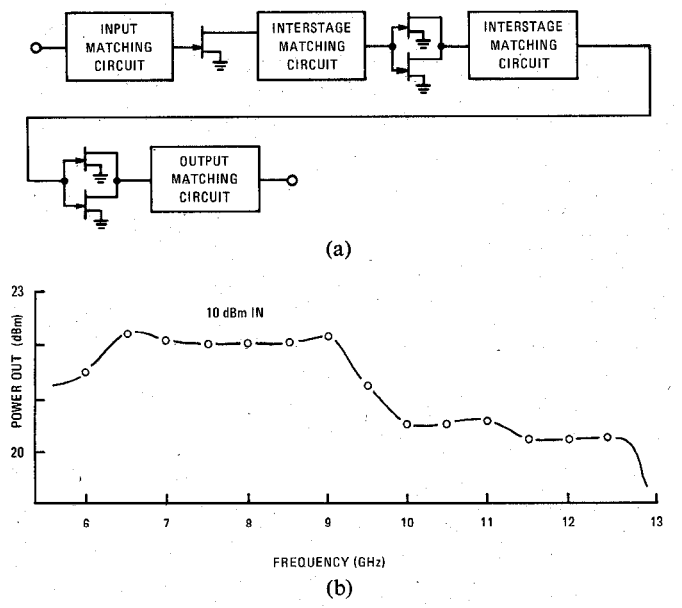

Fig. 7. Three-stage 100-mW 5.9–12.4-GHz amplifier. (a) Configuration. (b) Output power versus frequency at P_{in} = 10 dBm.

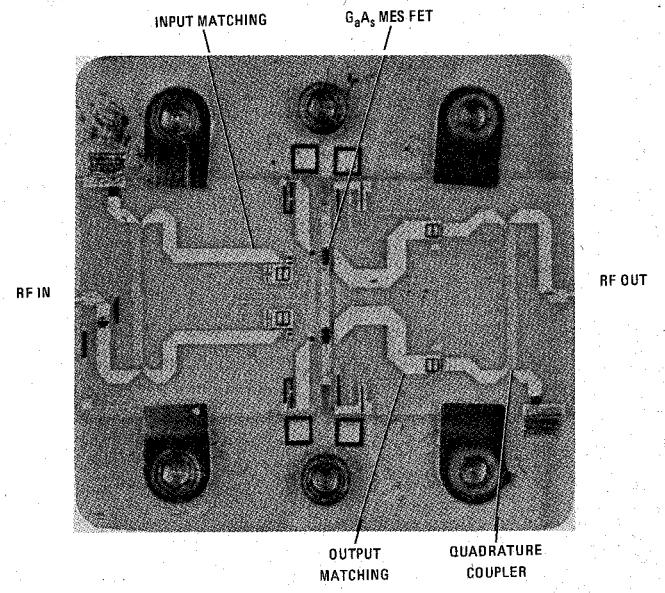

Fig. 8. MIC layout of 2–6.2-GHz 100-mW amplifier output stage.

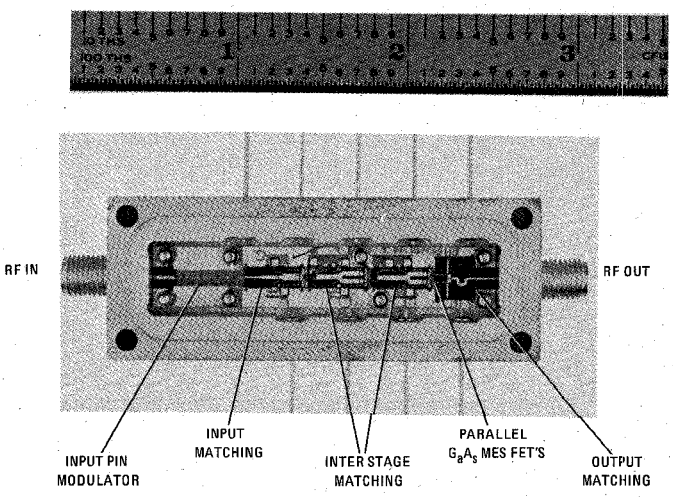

Fig. 9. Packaged 5.9–12.4 three-stage 100-mW GaAs MEFSET amplifier with p-i-n diode modulator at input.

10-dB gain at 100 mW. With proper large-signal matching structures, second-harmonic distortion was typically 30 dB below the fundamental at 100-mW outputs.

IV. Conclusion

The design of two GaAs MESFET amplifiers for extended bandwidths and medium power has been described. The device model and the stability considerations presented are typical of those faced in GaAs MESFET amplifier design. For small-signal matching, simplified *RC* equivalent input and output circuits for the MESFET have been shown to be useful for analytical design of matching structures as well as for rapid design optimization. A shunting technique has been described which facilitates design below 6 GHz. The large-signal load impedance for maximum gain has been determined as a function of power level and of frequency. Various power combining techniques have been compared. The final designs reflect the previously stated results, provid-

ing over 100 mW from 2–6.2 GHz and 5.9–12.4 GHz, respectively, with good match and ample gain.

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Wide-Band Gallium Arsenide Power MESFET Amplifiers

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Abstract—**The performance, with emphasis on wide bandwidth, that can be expected of linear medium power GaAs microwave MESFET (metal semiconductor field-effect-transistor) amplifiers is discussed. It starts with measured scattering parameters of devices and proceeds through computer-optimized device modeling, to amplifier circuit designs and performance results. It shows computed and measured octave bandwidth performance and reveals that decade bandwidth is feasible. It discusses single-ended and balanced amplifier design approaches. Some practical designs with performance results are presented, with circuit topologies which are easily realizable in microstrip.**

I. INTRODUCTION

MICROWAVE power MESFET's capable of approximately 1-W output power in the 4–9-GHz frequency range have been announced [1]–[3]. These results indicate significant progress in power FET technology leading to commercial availability in the near future. The Naval Research Laboratory has performed circuit computations and experimental amplifier construction using medium power, single-, and two-cell devices similar to those described in [3]. This paper reports the results of the investigation.

Section II gives general characteristics and modeling information on the devices used. Section III discusses the theoretical and practical bandwidth capability of devices and amplifiers. Section IV presents experimental results for single-ended and balanced amplifiers.

Manuscript received October 16, 1975; revised December 12, 1975. The MESFET devices were fabricated and characterized at RCA Laboratories, Princeton, NJ.

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II. GENERAL DEVICE CHARACTERISTICS

The configuration of the power MESFET flip-chip carrier is illustrated in Fig. 1. The chip's raised source pads are bonded to a pedestal formed as part of the carrier providing RF ground and heat sinking. The gate and drain connections are made with pairs (only one shown) of 0.0025-cm-diam bond wires to the metallized alumina standoff chips on both sides of the transistor chip. Additional cells may be